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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/593,891	06/14/2000	Sadao Nakayama	NFC DP-624	8215

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NORWAY P. SOLOWAY
HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AR 85701

EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/593,891	NAKAYAMA, SADAO	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communicati n appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 4, 2003 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on September 4, 2003 has been received and entered in the case.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Regarding claim 3, the drawings fail to show a combined structure that contains the following limitations in claims 1 and 3 "wherein the bonding pads on said upper chip that connect to the bonding pads of said substrate are disposed on **the lower surface of** said

upper chip" and a "**first bonding wire** for connecting the terminal of the surface of the upper chip with the first terminal" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. In other words, the drawings fail to show the upper chip is connected to the first terminal of the wiring substrate by flip chip (claim 1) and wiring bond (claim 3) when the wiring substrate is directly connected to the upper chip.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 3, the specification fails to disclose the combined structure of claims 1 and 3 that both structure a "flip chip bond" and "wiring bond" are formed between the upper chip and the substrate.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1, 2, 5, 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hikita et al. '637.

Regarding claim 1, Hikita et al. discloses in e.g., Fig. 39 and column 19, line 30 – column 20, line 19 a stacked semiconductor storage device comprising, in combination,

- a lower chip (17) and an upper chip (16) superimposed on a substrate (12a and 12b),
- said semiconductor storage device further comprising:
- a wiring substrate (14) having wiring patterns (e.g., 14a and 14b) thereon, interposed between and in direct contact with both said lower chip and said upper chip, for relaying electric connection (W, connected to the elements 14b) between bonding

pads on said upper chip (16) and bonding pads (at the connection area on the elements 12b) on said substrate (12a and 12b),

- wherein the bonding pads on said upper chip (16) are arranged in a line running perpendicular to a line of bonding pads (at the connection area on the elements 12b) on the substrate (12a and 12b);
- wherein said upper chip (16) has an upper and a lower surface, said lower surface facing said substrate; and
- wherein the bonding pads on said upper chip that connect to the bonding pads of said substrate are disposed on the lower surface of said upper chip.

Regarding claim 2, Hikita et al. discloses in e.g., Fig. 39 and column 19, line 30 – column 20, line 19 there being provided a first terminal (14a) connected to a terminal (16b) on a surface of the upper chip (16), a second terminal (14b) connected to a terminal (at the connection area on the elements 12b) on a surface of the substrate (12a and 12b), and a wiring pattern (column 19, lines 36 – 47) for connecting the first and the second terminals on the surface of the wiring substrate (14).

Regarding claim 5, Hikita et al. discloses in e.g., Fig. 39 and column 19, line 30 – column 20, line 19 said terminal (17a) of the surface of said lower chip (17) being connected to said terminal (at the connection area on the elements 12b) of the surface of said substrate (12a and 12b) by a third bonding wire (W attached to the element 17a).

Regarding claims 7 and 8, Hikita et al. discloses in e.g., Fig. 39 said wiring substrate bring sheet or board wiring substrate (14).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. in view of Takiar et al. '398.

Regarding claims 3, Hikita et al. discloses in e.g., Fig. 39 and column 19, line 30 – column 20, line 19 a semiconductor storage device further comprising: a second bonding wire (W, attached to the elements 14b) for connecting the terminal (at the connection area on the elements 12b) of the surface of the substrate (12a and 12b) with the second terminal (14b). However, Hikita et al. does not disclose a first bonding wire for connecting the terminal of the surface of the upper chip with the first terminal. Takiar et al. teaches in e.g., Fig. 4 a first bonding wire (wire attached to the elements 126 and 128) for connecting a terminal of the surface of an upper chip (128) with the first terminal (at the right-side of the terminal on the element 126). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Hikita et al. by using the first bonding wire as taught by Takiar et al. The ordinary artisan would have been motivated to modify Hikita et al. in the manner described above for at least the purpose of providing precise alignment, simple in cleaning and inspection and additional interconnections can be made (column 2, line 63 – column 3, line 4).

Regarding claims 4, Hikita et al. discloses in e.g., Fig. 39 and column 19, line 30 – column 20, line 19 a wiring pattern (14a and 14b) whose one end (14a) is connected to a terminal (16b) on a rear surface of the upper chip (16). However, Hikita et al. does not disclose a wiring pattern whose other terminal is connected to a terminal on a surface of the lower chip. Takiar et al. teaches in e.g., Fig. 4 a wiring pattern (the pad on the element 126) whose one end (at the one end of the pad on the element 126) is connected to a terminal of the upper chip (128) and whose other terminal is connected to a terminal (at the pad on the element 126) on a surface of a lower chip (124). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Hikita et al. by using the other end of the wiring pattern to connect to the terminal on the surface of the lower chip as taught by Takiar et al. The ordinary artisan would have been motivated to modify Hikita et al. in the manner described above for at least the purpose of decreasing shorting and reducing risks for wire sweep under fast mold transfer conditions or high resin viscosity (column 2, lines 33 – 41).

Regarding claim 6, Hikita et al. discloses in e.g., Fig. 39 and column 19, line 30 – column 20, line 19 said terminal (17a) of the surface of said lower chip (17) being connected to said terminal (at the connection area on the elements 12b) of the surface of said substrate (12a and 12b) by a third bonding wire (W attached to the element 17a).

Response to Arguments

10. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

c.c.
3/4/04 6:14:34 PM

BRADLEY BAUMEISTER
PRIMARY EXAMINER